AMENDMENT TO THE CLAIMS

Please amendment the claims, including all prior versions, with the listing of claims below.

Listing of the Claims:

1. (currently amended) An integrated circuit for video/audio processing that processes a video and audio signal, comprising:

a microcomputer including a CPU (central processor unit);

a stream input/output operable to receive/output a video and audio stream to and from an external device, under a control of said microcomputer;

a media processor operable to execute media processing including at least one of compression and decompression of the video and audio stream inputted to said stream input/output or outputted from said stream input/output under the control of said microcomputer;

an AV input/output operable to convert the video and audio stream subjected to the media processing in said media processor and output the video and audio stream to an a first external apparatus, or acquire the video and audio signal from the a second external apparatus and convert the video and audio signal into a video and audio stream subjected to the media processing in said media processor, under the control of said microcomputer; and

a memory interface operable to control a data transfer between a memory and said microcomputer, said stream input/output ~~block~~, said media processor and said AV input/output, under the control of said microcomputer, wherein

each of said microcomputer, said stream input/output, said media processor and said AV input/output is connected to and all data exchanged therebetween is through said memory interface by each of respective plural dedicated data buses,

each of the respective plural dedicated data buses is associated to one of said microcomputer, said stream input/output, said media processor and said AV input/output, and

the video and audio stream is exchanged through said memory among said microcomputer, said stream input/output, said media processor and said AV input/output.

2. (canceled).

3. (previously presented). The integrated circuit for video/audio processing according to Claim 1,

wherein said memory interface is operable to relay the data transfer so that the data transfer between said memory and said microcomputer, said stream input/output, said media processor and said AV input/output is made in parallel.

4. (previously presented). The integrated circuit for video/audio processing according to Claim 1,

wherein said microcomputer, said stream input/output, said media processor and said AV input/output have no buffer memory for buffering the video and audio stream.

5. (previously presented). The integrated circuit for video/audio processing according to Claim 1,

wherein said microcomputer, said stream input/output, said media processor and said AV input/output store the video and audio stream in said memory and notifies remaining ones of said stream input/output, said media processor and said AV input/output of the storage.

6. (previously presented). The integrated circuit for video/audio processing according to Claim 1,

wherein said stream input/output includes an interface operable to transmit and receive the video and audio stream to and from said external device, an encryption processor operable to encrypt or decrypt the transmitted and received video and audio stream, and a first direct memory access controller operable to transfer data between said external device and said memory,

said media processor including an instruction parallel processor which executes plural signal processing instructions in parallel, an accelerator which executes an arithmetic operation, and a second direct memory access controller operable to control the data transfer with said memory,

said AV input/output includes a graphics engine which executes graphics processing of image data, and a format converter operable to convert the format of the video signal, and

said memory interface includes plural ports connected to said microcomputer, said stream input/output, said media processor and said AV input/output, and has a memory scheduler which adjusts timing of data transfer at each of said plural ports.

7. (previously presented). The integrated circuit for video/audio processing according to Claim 6,

wherein said microcomputer further includes at least one of a clock controller operable to turn on/off a supply of a clock to said CPU and a power supply controller operable to turn on/off the power supply.

8. (previously presented). The integrated circuit for video/audio processing according to Claim 6,

wherein said media processor further includes a data parallel processor which executes an arithmetic operation on plural pieces of data in parallel.

9. (previously presented). The integrated circuit for video/audio processing according to Claim 1, further comprising:

a signal line which connects said stream input/output and said media processor,

wherein said media processor is operable to execute media processing of the video and audio stream inputted from said stream input/output through said signal line or the video and audio stream to be outputted to said stream input/output through said signal line.

10. (previously presented). The integrated circuit for video/audio processing according to Claim 1,

wherein circuit elements and wiring between said microcomputer, said stream input/output, said media processor, said AV input/output and said memory interface are formed on a circuit layer and a first wiring layer, respectively, on a semiconductor substrate; and

each of said plural dedicated data buses is formed on a second wiring layer located above said first wiring layer.

11. (previously presented). The integrated circuit for video/audio processing according to Claim 1,

wherein a structure of said integrated circuit is included in each of plural different system LSI (large-scale integration) corresponding to each of plural different devices; and

the plural different devices include at least two among a digital television, a digital video recorder, a video camera and a portable telephone.

12. (previously presented). The integrated circuit for video/audio processing according to Claim 11,

wherein assuming that one of said plural different devices is designated as a first device and another as a second device and a process is shared by said integrated circuit for video/audio processing for the first device and said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by said microcomputer of said integrated circuit for video/audio processing for the first device, the process is executed by said microcomputer of said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by said stream input/output of said integrated circuit for video/audio processing for the first device, the process is executed by said stream input/output of said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by said media processor of said integrated circuit for video/audio processing for the first device, the process is executed by said media processor of said integrated circuit for video/audio processing for the second device; and

in the case where the process is executed by said AV input/output of said integrated circuit for video/audio processing for the first device, the process is executed by said AV input/output of said integrated circuit for video/audio processing for the second device.

13. (previously presented). The integrated circuit for video/audio processing according to Claim 11,

wherein in the case where one of the plural different devices is designated as a first device and another as a second device,

the CPU of said integrated circuit for video/audio processing for the first device and the CPU of said integrated circuit for video/audio processing for the second device have instruction sets partially compatible with each other.

14. (previously presented). The integrated circuit for video/audio processing according to Claim 11,

wherein said media processing includes an instruction parallel processor which executes plural signal processing instructions in parallel; and

in the case where one of the plural different devices is designated as a first device and another as a second device,

the instruction parallel processor of said integrated circuit for video/audio processing for the first device and the instruction parallel processor of said integrated circuit for video/audio processing for the second device have instruction sets partially compatible with each other.

15. (currently amended). The integrated circuit for video/audio processing according to Claim 11,

wherein said media processor includes [[has]] an instruction parallel processor which executes plural signal processing instructions in parallel; and

in the case where one of the plural different devices is designated as a first device and another as a second device,

a core of the CPU of said integrated circuit for video/audio processing for the first device and a core of the CPU of said integrated circuit for video/audio processing for the second device have a same logic connection, and

a core of the instruction parallel processor of said integrated circuit for video/audio processing for the first device and a core of the instruction parallel processor of said integrated circuit for video/audio processing for the second device have a same logic connection.

16. (previously presented). The integrated circuit for video/audio processing according to Claim 11,

wherein said media processor includes an instruction parallel processor which executes plural signal processing instructions in parallel; and

in the case where one of the plural different devices is designated as a first device and another as a second device,

a core of the CPU of said integrated circuit for video/audio processing for the first device and a core of the CPU of said integrated circuit for video/audio processing for the second device have a same mask layout, and

a core of the instruction parallel processor of said integrated circuit for video/audio processing for the first device and a core of the instruction parallel processor of said integrated circuit for video/audio processing for the second device have a same mask layout.

17. (currently amended). The integrated circuit for video/audio processing according to Claim 11,

wherein in the case where one of the plural different devices is designated as a first device and another one is designated as a second device,

an address of a first control register for said stream input/output ~~block~~, said media processor, said AV input/output and said memory interface on a memory map of the CPU in said integrated circuit for video/audio processing for the first device is identical to an address of a second control register for said stream input/output, said media processor, said AV input/output and said memory interface on a memory map of the CPU in said integrated circuit for video/audio processing for the second device.

18. (previously presented). A method of designing and developing devices using the integrated circuit for video/audio processing according to Claim 1,

wherein the plural different devices include a digital television, a digital video recorder, a video camera and a portable telephone.

19. (previously presented). The method of designing and developing devices according to Claim 18, wherein the design and development is performed in such a manner that:

assuming that one of the plural different devices is designated as a first device and another of the plural different devices is designated as a second device and a process is shared by said integrated circuit for video/audio processing for the first device and said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by a microcomputer of said integrated circuit for video/audio processing for the first device, the process is executed by a microcomputer of said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by a stream input/output of said integrated circuit for video/audio processing for the first device, the process is executed by a stream input/output of said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by a media processor of said integrated circuit for video/audio processing for the first device, said process is executed by a media processor of said integrated circuit for video/audio processing for the second device; and

in the case where the process is executed by an AV input/output of said integrated circuit for video/audio processing for the first device, the process is executed by an AV input/output of said integrated circuit for video/audio processing for the second device.

20. (previously presented). The integrated circuit for video/audio processing according to Claim 1,

wherein said AV input/output is further operable to generate a recording video signal by converting a resolution of the video signal converted from a video stream subjected to media processing by said media processor or acquired from said second external apparatus, as well as generating field feature information indicating at least one of in-field total and inter-field difference of video fields indicated by the recording video signal; and

said media processor is further operable to access the field feature information and convert the recording video signal into a recording video stream.

21. (previously presented). The integrated circuit for video/audio processing according to Claim 20, further comprising:

a signal line which connects said media processor and said AV input/output,

wherein the field feature information is exchanged between said media processor and said AV input/output through said signal line.

22. (previously presented). The integrated circuit for video/audio processing according to Claim 1,

wherein said media processor executes, by time division, a multiplexing or demultiplexing process for the video and audio stream, a video data compressing or decompressing process, and an audio data compressing or decompressing process for one video/audio multiplex stream, as well as prohibiting the multiplexing or demultiplexing process

23. (previously presented). The integrated circuit for video/audio processing according to Claim 22,

wherein said media processor includes a virtual multiprocessor functioning as plural logical processors by time division;

the multiplexing or demultiplexing process for said video and audio stream, the compressing or decompressing process for said video data, and the compressing or decompressing process for said audio data are executed by different logical processors, respectively, which are a function of said virtual multiprocessor; and

a logical processor for executing the multiplexing or demultiplexing process for said video and audio stream sleeps until an expiration of a time on a predetermined timer after completion of the processing of a predetermined unit of said video and audio stream.

24. (currently amended). An integrated circuit for video/audio processing that processes a video and audio signal, comprising:

a microcomputer including a CPU (central processing unit);

a stream input/output operable to receive/output a video and audio stream to and from an external device, under a control of said microcomputer;

a media processor operable to execute media processing including at least one of compression and decompression of the video and audio stream inputted to said stream input/output or outputted from said stream input/output ~~block~~ under the control of said microcomputer;

an AV input/output operable to convert the video and audio stream subjected to the media processor in said media processor and output the video and audio stream to a first external apparatus, or acquire the video and audio signal from a second external apparatus and convert the video and audio signal into a video and audio stream to be subjected to the media processing in said media processor, under the control of said microcomputer;

a memory interface operable to control a data transfer between a memory and said microcomputer, said stream input/output, said media processor and said AV input/output, under the control of said microcomputer; and

plural dedicated data buses, each dedicated data bus of said plural dedicated data buses directly connecting and all data exchanged therebetween is through said memory interface to a

respective one of each of said microcomputer, said stream input/output, said media processor and said AV input/output, wherein

each dedicated data bus of said plural dedicated data buses being associated to one of said microcomputer, said stream input/output, said media processor and said AV input/output, and

the video and audio stream is exchanged through said memory among said microcomputer, said stream input/output, said media processor and said AV input/output.

25. (previously presented). The integrated circuit for video/audio processor according to claim 24, wherein each dedicated data bus of the plural dedicated data buses connects said memory interface with only each of said microcomputer, said stream input/output, said media processor and said AV input/output at all times.

26 (new). An integrated circuit for video/audio processing that processes a video and audio signal, comprising:

a microcomputer including a CPU (central processor unit);

a stream input/output operable to receive/output a video and audio stream to and from an external device, under a control of said microcomputer;

a media processor operable to execute media processing including at least one of compression and decompression of the video and audio stream inputted to said stream input/output or outputted from said stream input/output under the control of said microcomputer;

an AV input/output operable to convert the video and audio stream subjected to the media processing in said media processor and output the video and audio stream to an a first external apparatus, or acquire the video and audio signal from the a second external apparatus and convert

the video and audio signal into a video and audio stream subjected to the media processing in said media processor, under the control of said microcomputer; and

a memory interface operable to control a data transfer between a memory and said microcomputer, said stream input/output, said media processor and said AV input/output, under the control of said microcomputer, wherein

each of said microcomputer, said stream input/output, said media processor and said AV input/output is connected to said memory interface by each of respective plural dedicated data buses,

when data is transferred between any two of said microcomputer, said stream input/output, said media processor and said AV input/output, all transferred data is exchanged through said memory interface,

each of the respective plural dedicated data buses is associated to one of said microcomputer, said stream input/output, said media processor and said AV input/output, and

the video and audio stream is exchanged through said memory among said microcomputer, said stream input/output, said media processor and said AV input/output.

27. (new). The integrated circuit for video/audio processing according to Claim 26,

wherein said memory interface is operable to relay the data transfer so that the data transfer between said memory and said microcomputer, said stream input/output, said media processor and said AV input/output is made in parallel.

28. (new). The integrated circuit for video/audio processing according to Claim 26,

wherein said microcomputer, said stream input/output, said media processor and said AV input/output have no buffer memory for buffering the video and audio stream.

29. (new). The integrated circuit for video/audio processing according to Claim 26,

wherein said microcomputer, said stream input/output, said media processor and said AV input/output store the video and audio stream in said memory and notifies remaining ones of said stream input/output, said media processor and said AV input/output of the storage.

30. (new). The integrated circuit for video/audio processing according to Claim 26,

wherein said stream input/output includes an interface operable to transmit and receive the video and audio stream to and from said external device, an encryption processor operable to encrypt or decrypt the transmitted and received video and audio stream, and a first direct memory access controller operable to transfer data between said external device and said memory,

said media processor including an instruction parallel processor which executes plural signal processing instructions in parallel, an accelerator which executes an arithmetic operation, and a second direct memory access controller operable to control the data transfer with said memory,

said AV input/output includes a graphics engine which executes graphics processing of image data, and a format converter operable to convert the format of the video signal, and

said memory interface includes plural ports connected to said microcomputer, said stream input/output, said media processor and said AV input/output, and has a memory scheduler which adjusts timing of data transfer at each of said plural ports.

31. (new). The integrated circuit for video/audio processing according to Claim 30,

wherein said microcomputer further includes at least one of a clock controller operable to turn on/off a supply of a clock to said CPU and a power supply controller operable to turn on/off the power supply.

32. (new). The integrated circuit for video/audio processing according to Claim 30,

wherein said media processor further includes a data parallel processor which executes an arithmetic operation on plural pieces of data in parallel.

33. (new). The integrated circuit for video/audio processing according to Claim 26, further comprising:

a signal line which connects said stream input/output and said media processor,

wherein said media processor is operable to execute media processing of the video and audio stream inputted from said stream input/output through said signal line or the video and audio stream to be outputted to said stream input/output through said signal line.

34. (new). The integrated circuit for video/audio processing according to Claim 26,

wherein circuit elements and wiring between said microcomputer, said stream input/output, said media processor, said AV input/output and said memory interface are formed on a circuit layer and a first wiring layer, respectively, on a semiconductor substrate; and

each of said plural dedicated data buses is formed on a second wiring layer located above said first wiring layer.

35. (new). The integrated circuit for video/audio processing according to Claim 26,

wherein a structure of said integrated circuit is included in each of plural different system LSI (large-scale integration) corresponding to each of plural different devices; and

the plural different devices include at least two among a digital television, a digital video recorder, a video camera and a portable telephone.

36. (new). The integrated circuit for video/audio processing according to Claim 35,

wherein assuming that one of said plural different devices is designated as a first device and another as a second device and a process is shared by said integrated circuit for video/audio processing for the first device and said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by said microcomputer of said integrated circuit for video/audio processing for the first device, the process is executed by said microcomputer of said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by said stream input/output of said integrated circuit for video/audio processing for the first device, the process is executed by said stream input/output of said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by said media processor of said integrated circuit for video/audio processing for the first device, the process is executed by said media processor of said integrated circuit for video/audio processing for the second device; and

in the case where the process is executed by said AV input/output of said integrated circuit for video/audio processing for the first device, the process is executed by said AV input/output of said integrated circuit for video/audio processing for the second device.

37. (new). The integrated circuit for video/audio processing according to Claim 35,

wherein in the case where one of the plural different devices is designated as a first device and another as a second device,

the CPU of said integrated circuit for video/audio processing for the first device and the CPU of said integrated circuit for video/audio processing for the second device have instruction sets partially compatible with each other.

38. (new). The integrated circuit for video/audio processing according to Claim 35,

wherein said media processing includes an instruction parallel processor which executes plural signal processing instructions in parallel; and

in the case where one of the plural different devices is designated as a first device and another as a second device,

the instruction parallel processor of said integrated circuit for video/audio processing for the first device and the instruction parallel processor of said integrated circuit for video/audio processing for the second device have instruction sets partially compatible with each other.

39. (new). The integrated circuit for video/audio processing according to Claim 35,

wherein said media processor includes an instruction parallel processor which executes plural signal processing instructions in parallel; and

in the case where one of the plural different devices is designated as a first device and another as a second device,

a core of the CPU of said integrated circuit for video/audio processing for the first device and a core of the CPU of said integrated circuit for video/audio processing for the second device have a same logic connection, and

a core of the instruction parallel processor of said integrated circuit for video/audio processing for the first device and a core of the instruction parallel processor of said integrated circuit for video/audio processing for the second device have a same logic connection.

40. (new). The integrated circuit for video/audio processing according to Claim 35,

wherein said media processor includes an instruction parallel processor which executes plural signal processing instructions in parallel; and

in the case where one of the plural different devices is designated as a first device and another as a second device,

a core of the CPU of said integrated circuit for video/audio processing for the first device and a core of the CPU of said integrated circuit for video/audio processing for the second device have a same mask layout, and

a core of the instruction parallel processor of said integrated circuit for video/audio processing for the first device and a core of the instruction parallel processor of said integrated circuit for video/audio processing for the second device have a same mask layout.

41. (new). The integrated circuit for video/audio processing according to Claim 35,

wherein in the case where one of the plural different devices is designated as a first device and another one is designated as a second device,

an address of a first control register for said stream input/output, said media processor, said AV input/output and said memory interface on a memory map of the CPU in said integrated circuit for video/audio processing for the first device is identical to an address of a second control register for said stream input/output, said media processor, said AV input/output and said memory interface on a memory map of the CPU in said integrated circuit for video/audio processing for the second device.

42. (new). A method of designing and developing devices using the integrated circuit for video/audio processing according to Claim 26,

wherein the plural different devices include a digital television, a digital video recorder, a video camera and a portable telephone.

43. (new). The method of designing and developing devices according to Claim 42, wherein the design and development is performed in such a manner that:

assuming that one of the plural different devices is designated as a first device and another of the plural different devices is designated as a second device and a process is shared by said integrated circuit for video/audio processing for the first device and said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by a microcomputer of said integrated circuit for video/audio processing for the first device, the process is executed by a microcomputer of said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by a stream input/output of said integrated circuit for video/audio processing for the first device, the process is executed by a stream input/output of said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by a media processor of said integrated circuit for video/audio processing for the first device, said process is executed by a media processor of said integrated circuit for video/audio processing for the second device; and

in the case where the process is executed by an AV input/output of said integrated circuit for video/audio processing for the first device, the process is executed by an AV input/output of said integrated circuit for video/audio processing for the second device.

44. (new). The integrated circuit for video/audio processing according to Claim 26,

wherein said AV input/output is further operable to generate a recording video signal by converting a resolution of the video signal converted from a video stream subjected to media processing by said media processor or acquired from said second external apparatus, as well as generating field feature information indicating at least one of in-field total and inter-field difference of video fields indicated by the recording video signal; and

said media processor is further operable to access the field feature information and convert the recording video signal into a recording video stream.

45. (new). The integrated circuit for video/audio processing according to Claim 44, further comprising:

a signal line which connects said media processor and said AV input/output,

wherein the field feature information is exchanged between said media processor and said AV input/output through said signal line.

46. (new)The integrated circuit for video/audio processing according to Claim 26,

wherein said media processor executes, by time division, a multiplexing or demultiplexing process for the video and audio stream, a video data compressing or decompressing process, and an audio data compressing or decompressing process for one video/audio multiplex stream, as well as prohibiting the multiplexing or demultiplexing process

47. (new). The integrated circuit for video/audio processing according to Claim 46,

wherein said media processor includes a virtual multiprocessor functioning as plural logical processors by time division;

the multiplexing or demultiplexing process for said video and audio stream, the compressing or decompressing process for said video data, and the compressing or decompressing process for said audio data are executed by different logical processors, respectively, which are a function of said virtual multiprocessor; and

a logical processor for executing the multiplexing or demultiplexing process for said video and audio stream sleeps until an expiration of a time on a predetermined timer after completion of the processing of a predetermined unit of said video and audio stream.